Reaching saturation in patterned source vertical organic field effect transistors

Michael Greenman,1 Gil Sheleg,1 Chang-min Keum,2 Jonathan Zucker,1 Bjorn Lussem,2 and Nir Tessier1,a)
1Sara and Moshe Zisapel Nano-Electronic Center, Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa 32000, Israel
2Department of Physics, Kent State University, Kent, Ohio 44242, USA

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Like most of the vertical transistors, the Patterned Source Vertical Organic Field Effect Transistor (PS-VOFET) does not exhibit saturation in the output characteristics. The importance of achieving a good saturation is demonstrated in a vertical organic light emitting transistor; however, this is critical for any application requiring the transistor to act as a current source. Thereafter, a 2D simulation tool was used to explain the physical mechanisms that prevent saturation as well as to suggest ways to overcome them. We found that by isolating the source facet from the drain-source electric field, the PS-VOFET architecture exhibits saturation. The process used for fabricating such saturation-enhancing structure is then described. The new device demonstrated close to an ideal saturation with only 1% change in the drain-source current over a 10 V change in the drain-source voltage. Published by AIP Publishing.

I. INTRODUCTION

The demand for low-cost thin-film transistor (TFT) has been growing in the past years driven by/along with the increased interest in wearable electronic and internet of things. For many applications, single crystalline silicon transistors are too complex to integrate, too expensive, and lack the potential for flexibility. The current TFT technologies (such as amorphous silicon or metal oxides) are not yet fully meeting the applications’ need regarding uniformity and stability1,2 and compatibility for flexible substrates. Organic Field Effect Transistors (OFETs) are one possible candidate for TFT.3–5 However, the relatively low mobilities of organic semiconductors (OSCs) prevent commercializing the conventional lateral OFETs. Shortening the channel length to compensate for the low mobilities led to new structures of OFETs;6–10 some are known as Vertical OFETs (VOFETs).11,12 Several reports suggest that the vertical FETs and specifically the patterned source VOFETs13–25 have the potential for better performance compared with the lateral one. Another key advantage of the vertical design is that an organic light emitting diode (OLED) can be fabricated right on top of the transistor, which allow for a large fill factor in active matrix OLED (AMOLED) displays.26–31

The PS-VOFET is formed by stacking several layers (see Fig. 1). This vertical architecture approach allows to define a short channel in the transistor using low-cost and simple fabrication process. The PS-VOFET16 design relies on holes in the source electrode to allow the electric field from the gate to reduce the injection barrier, at the source/organic semiconductor interface, and draw current from the source such that a vertical channel can be formed. Once the injection is enabled by the gate, carriers can accumulate at the interface, between the gate dielectric and the OSC, followed by drift towards the drain electrode.32 Detailed analysis of structural parameters has provided analytical expressions33 as well as design rules,32 which identified the top surface of the source electrode as the off or leakage area34 and suggested to use a multilayer source electrode with the top surface used to block the leakage.32 This multilayer approach was used to demonstrate high quality VOFETs.18 An experimental comparison of two VOFETs, with and without the leakage blocking layer, showed that the blocking layer reduced the leakage by 3 orders of magnitude, which made it possible to build inverter circuits.32 Introducing a buried organic layer18 offered better flexibility in device design, a feature we use here as well.

In this work, we describe the fabrication of an OLED on top PS-VOFET, a structure known as vertical organic light emitting transistor (VOLET).26–30 However, similar to other works, the improvement in current densities, using a shorter channel, generates a new challenge: reaching drain saturation regime. Saturation regime is essential for all applications where transistors are used as current sources, in particular, for AMOLED displays where it is important to maintain a fixed current (brightness) even at the expense of higher voltage operation of the pixel’s OLED. We discuss the inherent structure fault preventing the drain saturation regime and study an improved structure to reach saturation. We do so by both simulating and fabricating the two structures.

II. VOLET AND THE NEED FOR SATURATION IN OUTPUT CHARACTERISTICS

To demonstrate the potential of the PS-VOFET, VOLETs were fabricated by stacking a p-i-n type OLED on top of a PS-VOFET. N-type devices were fabricated with a structure similar to a previous report22 but without the drain electrode.
and with a thinner organic semiconductor (OSC) layer (200 nm instead of 300 nm). The fabrication was completed by adding the light emitting structure on top of the PS-VOFET. The resulting device structure is shown in Fig. 2(b), and the fabrication process is detailed in Sec. II. Images of the fabricated devices are shown in Figs. 2(c) and 2(d), which show the VOLET in its off ($V_G = -20\ V$) and on state ($V_G = 30\ V$), respectively. Figure 2(e) shows the electroluminescent spectrum of the VOLET.

In this structure, the PS electrode is used as an electron injecting contact for the OLED and the gate modulates this electron injection. Due to the p-doped hole transport layer (HTL), hole injection is ohmic. Since the silicon substrate is not transparent, a thin silver anode (20 nm) was used as semi-transparent contact. Measured luminance and current of this device are presented in Fig. 2(a). For constant and positive anode-cathode (drain-source) voltage, the gate modulates both the current and the light output. The data in Fig. 2(a) highlight two challenges associated with such device structures. First, the off current is dependent on the drain-source voltage and is relatively high, leading to power loss when the device should be off. Second, across the entire bias range, the drain-source current and the luminance are strongly affected by the drain-source voltage and not only by the gate. The device current is increasing by 200% when the drain voltage is increased by 30%. It was suggested that the same mechanism causes these two phenomena. The source electrode side walls are exposed to the electric field from the drain, thus allowing the drain to partially act in a similar manner to the gate electrode.

### III. PS-VOFET STRUCTURE THAT SUPPORTS SATURATION

The first PS-VOFET that we reported in 2009 was fabricated using an unconventional block copolymer lithography. The advantage of that process was the high density of holes in the PS electrode, thus enabling high currents (3 A cm$^{-2}$) even for low mobility ($10^{-3}\ \text{cm}^2/\text{V s}$) material. However, manipulation of the source electrode structure and addition of a source insulator are better controlled using more conventional methods such as shadow mask or photo-lithography. Naturally, the use of larger scale lithography results in lower current densities, an issue that will not be addressed here.

### A. Simulation results

To better understand the reason for the lack of saturation in the vertical transistor and to define a strategy to optimize the PS-VOFETs, we compare three device structures. In the first structure, direct source-drain leakage is suppressed by an insulator on top of the source [Fig. 3(a)]. In this structure, the gate draws charges from the source similarly to conventional lateral bottom contact OFETs. In the second structure, a thin semiconducting layer is added between the source and gate, making the PS similar to lateral top contact OFETs [Fig. 3(b)]. In such a structure, the current can be injected along the whole source electrode/OSC interface, to partially compensate for the injection barrier. Finally, in a third structure, the side-walls of the source electrode are covered as well [Fig. 3(c)].

These device structures were modeled in COMSOL using semiconductor module. The built-in 2D (x, z) semiconductor module was modified to account for the barrier lowering effect of the image potential (force). We simulated one unit cell [see Figs. 3(a)–3(c)] with a total width of 4 μm and a...

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**FIG. 1.** Schematic description of the PS-VOFET structure reported in Ref. 16. (a) 3D device structure with a cylindrical active cell. (b) 2D cross section of the device active cell with the layers’ notations.

**FIG. 2.** (a) Transfer and luminance characteristics of the VOLET with PS electrode. The solid lines refer to the drain-source current and the dashed lines refer to the luminance. (b) Simplified layer structure of PS based VOLET. (c) and (d) Camera pictures of the VOLET under constant drain bias, $V_{DS} = 19\ V$, at $V_G = -20\ V$ and $V_G = 30\ V$, respectively. (e) Electroluminescence spectrum of the VOLET. TL and BL stand for transport and blocking layer, respectively. H and E stand for hole and electron, respectively.
hole size of 2 μm. In the structure shown in Fig. 3(c), the side wall coverage, by insulator, was 50 nm. The device height (gate insulator to drain) was 210 nm without buried OSC layer and 260 nm with buried OSC layer. Using the literature data, the electron mobility was taken to be 0.1 cm² V⁻¹ s⁻¹, and the source electrode injection barrier was 0.7 eV, assuming the gold work-function to be 5 eV and PTCDI-C8 LUMO level at 4.3 eV.²²

The simulations results in Figs. 3(d) and 3(e) show that in both cases, where the patterned source is designed either as bottom gate bottom electrodes or bottom gate top electrode, the absolute currents are similar and, most importantly, the current does not saturate at any drain bias. In fact, the original design of the PS-VOFET³² was such that the gate bias creates a virtual ohmic-electrode, thus turning the source drain diode into a space charge limited (SCL) one. The inset to Fig. 3(d) presents the data in log-log scale, which indeed exhibit a power law of ~2, characteristic of SCL. Covering the edges of the source, as shown in Figs. 3(c) (structure) and 3(f) (simulated characteristics), leads to substantial changes in the output characteristic. By covering the edge of the source, no facet of the source is exposed to the drain potential and hence the drain current saturates at higher drain voltages. Overall, the current increases by only 6% for a change of V_DS from 15 V to 18 V. However, as we effectively shield the source electrode from the drain potential, the maximum achievable current density drops from 4.5 × 10⁻¹ A cm⁻² to 10⁻³ A cm⁻².

B. Experimental results

The above modeling result is verified experimentally by comparing the two device structures shown in Fig. 4. In the structure shown in Fig. 4(a),²² the source electrode consists of gold with two thin adhesion layers, titanium and aluminum, to ensure a good adhesion of the bottom and top oxides, respectively. The PS-OSC interface, gold and PTCDI-C8 in this case, is at the heart of this PS-VOFET structure. Gold and PTCDI-C8 layers are chosen, because they provide a high injection barrier and ensure that the gate-source electric field is required to lower the injection barrier and to switch the transistor on.³² However, as discussed above, the PS-OSC interface is also exposed to the electric field associated with the drain [red arrows in Fig. 4(a)], i.e., the injection of carriers is affected by a large drain-source bias as well. As suggested by the simulation, the side walls as well as the top of the PS were covered with SiO₂ in order to reach saturation [Fig. 4(b)]. Furthermore, a thin PTCDI-C8 layer is included between the source and gate electrode to make the PS similar to lateral top contact OFETs. The devices were patterned by lift-off resist (LOR) suited for OSCs.¹⁸,³⁷

Developing the fabrication process of these structures, we noted that the insulators did not always provide the improved performance predicted by the simulations. Hence, the process steps were adjusted with the aid of cross-sectional images of scanning electron microscopy (SEM). The SEM images of the final, and successful, structures are shown in Figs. 4(c) and 4(d). Specifically, in these devices, the lift-off is clean with no residual protruding metal that would act as leakage-enhancing spikes. Also, Fig. 4(d) shows that the e-beam evaporated amorphous SiO₂ fully covers the source top and side facets.

In Fig. 5, we compare the measured output characteristics of the two structures shown in Fig. 4. Figure 5(a) shows...
the typical output characteristics\textsuperscript{22} of the PS-VOFET structure depicted in Figs. 4(a) and 4(c) and simulated in Fig. 3(d). As shown in the inset to Fig. 5(a), the current dependence on the drain-source bias is a power law of $\sim 2$, indicating that the virtual ohmic-contact was formed to support SCL current. The measured output characteristics of the structure that should enhance the saturation behavior [covered sidewalls, Figs. 4(b) and 4(d)] are shown in Fig. 5(b). In accordance with the simulations [Fig. 3(f)], a saturation, in the current as a function of the drain-source bias, is clearly visible. For a gate voltage of 20 V and a drain voltage between 6 and 14 V, the total change in drain-source current is less than 5%.

To complete the discussion, the transfer characteristics of the structure shown in Figs. 4(b) and 4(d) are plotted in semi-log scale in Fig. 6(a). The transfer characteristics are shown as measured in the forward (solid line) and backward (dashed line) directions. Although some hysteresis is visible, the difference between the forward and backward sweep is rather low. The overlap of the curves for small values of gate bias is another manifestation of the existence of saturation in the output characteristics. The saturation observed as a function of gate bias is typical for this type of vertical FETs.\textsuperscript{32} Once the gate has fully enabled the injection from the patterned source, the current of the PS-VOFET does not change even if the gate bias is enhanced. However, the devices discussed here show significant gate-leakage currents, plotted in black curves in Fig. 6(a). Although these leakage currents are typically at least an order of magnitude lower than the drain-source current, they limit the on/off ratio to about $10^5$. In our experience, this level of leakage is largely due to the processing procedure that was not optimized enough for this aspect. Figure 6(b) shows the output characteristics presented in Fig. 5(b) but on linear scale. It clearly shows that on this more relevant scale, the performance is better but still not fully sufficient. In Fig. 6(c), we show the output characteristic of a different PS-VOFET produced using the same process. The saturation for this saturation-enhanced PS-VOFET is almost ideal. At a gate bias of 30 V, there is a current change of less than 1% over 10 V change in $V_{DS}$ (7–17 V).

IV. SUMMARY

A VOLET based on PS-VOFETs was presented. The absence of a drain saturation regime in the VOLET is a direct result of the transistor structure.\textsuperscript{22} Using 2D drift-diffusion simulations, we found that the lack of drain current saturation is caused by the influence of the drain voltage on the injection at the edges of the source electrode. An optimized device-structure was presented, where an additional organic layer is included between the source electrode and gate insulator and where the edges of the source electrode are covered with an insulator. It is shown that, by both simulation and experiment, the newer structure leads to drain current saturation in the output characteristics, but at the expense of reduction in the currents.

Based on our experience, extra effort is required to ensure that all the structural features remain intact over large areas, since patterning on top of organic layers by lithography is not well developed yet. Once this is achieved, a good agreement between simulation and measurements is achieved. In some
cases, the measured devices perform better than those predicted by simulations.

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APPENDIX: FABRICATION

1. VOLET

The PS was fabricated as described in a previous report. On top of the PS, a 200 nm of N,N-dioctyl-3,4,9,10 perylenedicarboximide (PTCDI-C8, 99.5%) was evaporated. The remaining VOLET fabrication process was completed at Kent State University (OH) by depositing a p-i-n OLED on top. Note that the samples were stored in a closed gel-box to prevent air exposure while being transported to Kent State University. From the bottom to top, the following layers were deposited: 2,9-bis(naphthalen-2-yl)-4,7-diphenyl-1,10-phenanthroline (NBphen, purity >99%) (70 nm) doped with cesium carbonate (Cs2CO3 99% Sigma-Aldrich) at 5 wt. % as electron transport layer (ETL), bis(2-methyl-8-quinolinolate)-4-(phenylphenolato)aluminum (BAIq, >99%) (10 nm) as a hole blocking layer (HBL), N,N’-bis(naphthalen-1-yl)-N,N’-bis(phenyl)benzidine (NPB, >99.5) doped with the phosphorescent emitter, bis(2-methyl-9-phenylbenzof[1,2-b:4,5-b]dioxazole) (acetylacetonate)iridium(III) [Ir(MDQ)2(acac), >99%] as emission layer (EML) (20 nm), NPB (10 nm) as an electron blocking layer (EVL), 2,2’,7,7’-tetrakis-(N,N-di-methylphenylamino)-9,9-spiro-bifluorene (Spiro-TTB >99%) (60 nm) doped with 2,2’-(perfluoronaphthalene-2,6-diylidene)dimalononitrile (F6-TCNNQ) at 4 wt. %, as holes transport layer (HTL), and finally Ag (20 nm) as a semitransparent top electrode. The organic materials, except Cs2CO3, were purchased from Lumtec Corp., and all materials were used without further purification. The OLED layers were deposited by thermal evaporation in a vacuum chamber (Angstrom Engineering, Inc.) at a base pressure of 1 × 10⁻⁷ Torr and structured by shadow masks defining an effective emission area of 1 × 1 mm². The doped layers were prepared by co-evaporation; the precise doping concentration is controlled by the evaporation rates. Each deposition rate was individually monitored with two quartz crystal microbalances. The electrical and optical characteristics of our top-emission VOLET were simultaneously measured using a semiconductor parameter analyzer (4200-SCS, Keithley) and a photodiode (FDS1010, Thorlab) in a nitrogen-filled glove box under a dark ambient condition. The electroluminescence spectrum of the Ir(MDQ)2(acac) emission was obtained using a spectrometer (USB4000, OceanOptics) and an integrating sphere (FOIS-1, OceanOptics) coupled to an optical fiber (OceanOptics).

B. PS-VOFET with saturation enhancing structure

The devices were fabricated on a highly doped 4-in. silicon wafer with 100 nm thick thermal oxide (prime grade, Nova Electronic Materials). The doped silicon and SiO2 layers were used as a gate electrode and a gate dielectric, respectively. The fabrication process started with the evaporation of the first OSC layer, 50 nm of PTCDI-C8. On top of the first OSC spin-coat, a special lift-off resist (LOR) designed to be compatible with organic materials (OCoR SL1, Orthogonal). After a short drying (1 min, 100°C), a conventional photoresist (5214, AZ Electronics Materials) was applied. To generate the pattern of array of round holes (see Fig. 1 and Ref. 22), we used a reversal image process (MA-6 contact mask aligner, SUSS) to transfer the pattern to the photoresist. Next, the LOR was developed (spin puddle, Developer 100, Orthogonal), and a clear undercut was achieved. 25 nm gold layer followed by 3 nm of aluminum were thermally evaporated and used as a source electrode. A layer of 65 nm SiO2 was evaporated, using e-beam, as a source insulator. The use of LOR enabled to generate a deeper undercut (negative slope) below the photoresist through over developing the LOR. With this undercut, it is possible to use more isotropic SiO2 deposition to cover the source sidewalls. The evaporation chamber (PVD-20 by VINCI) is tall enough to minimize e-beam induced damage to the photoresist. The fabrication of PS was completed by the complete removal of the LOR (Striper 700, Orthogonal).
The second layer of OSC was also thermally evaporated (300 nm, PTCDI-C8). The devices were completed by thermal evaporation of aluminum drain electrode. The size of all measured devices in this report is 1 mm × 1 mm.

The electrical measurements were carried out using Semiconductor Parameter Analyzer (Agilent 4155B) and performed inside a glove box to extended device lifetime. Although silicon is not a flexible substrate, all the fabrication steps were made at low-temperatures making them plastic substrate compatible.